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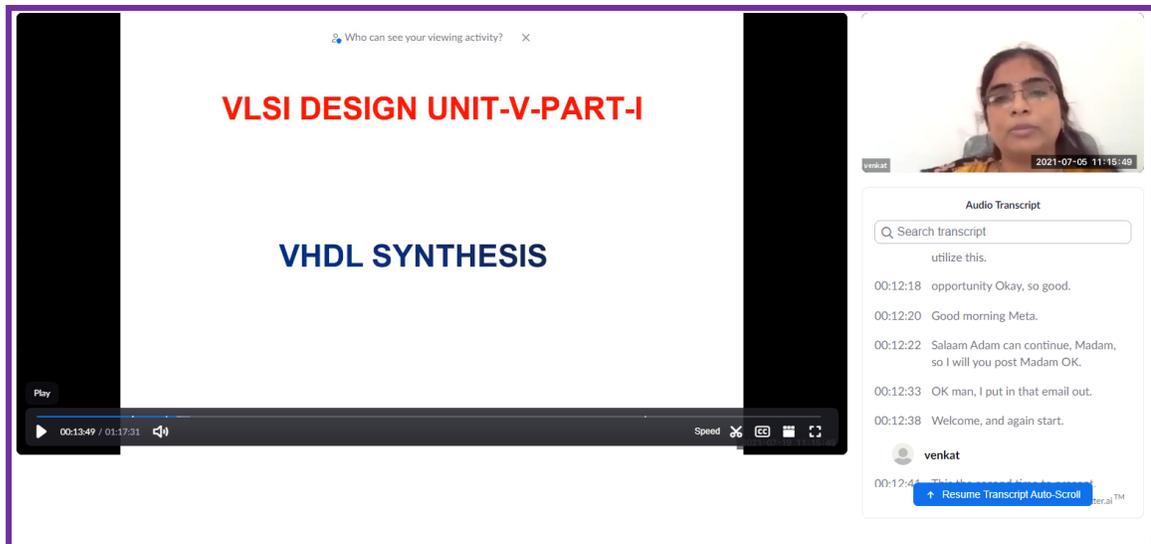
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

1	Name of the Activity/Event	Guest Lecture on “ VLSI Design ”		
2	Date of Activity/Event	05/07/2021 to 14/07/2021		
3	Organized by	Department of Electronics And Communication Engineering		
4	Place of Activity/event	Online		
5	Resource persons / guest / organization	G. Sarala, Intel corporation, Project lead, Bangalore		
6	Type of activity/Event	Guest Lecture		
7	Activity/Event objectives	<ul style="list-style-type: none"> This course aims at providing an opportunity for students to enrich their knowledge and skill in developing various solutions for solving engineering problems in the society. This program serves as a platform for students to work with the recent trends in Electronic simulation related areas. 		
8	Participation	Students	Faculty	Total Participation
		123	-	123
9	General remarks	<ol style="list-style-type: none"> 1. Introduction to VHDL 2. Subsystem design 3. FPGA and CPLDs 		
10	Suggested Improvements	Need Hands-on session and more real time examples.		
11	Enclosures	<ol style="list-style-type: none"> 1. Program report with Snapshots 2. Attendance sheet 		
12	Signature of Co-ordinator			

The **Electronics and Communication Engineering** department has organized a **Guest Lecture** on “VLSI Design” from **05/07/2021 to 14/07/2021**, The Resource person is **Mrs. G. Sarala, Intel corporation, Project lead, Bangalore.**

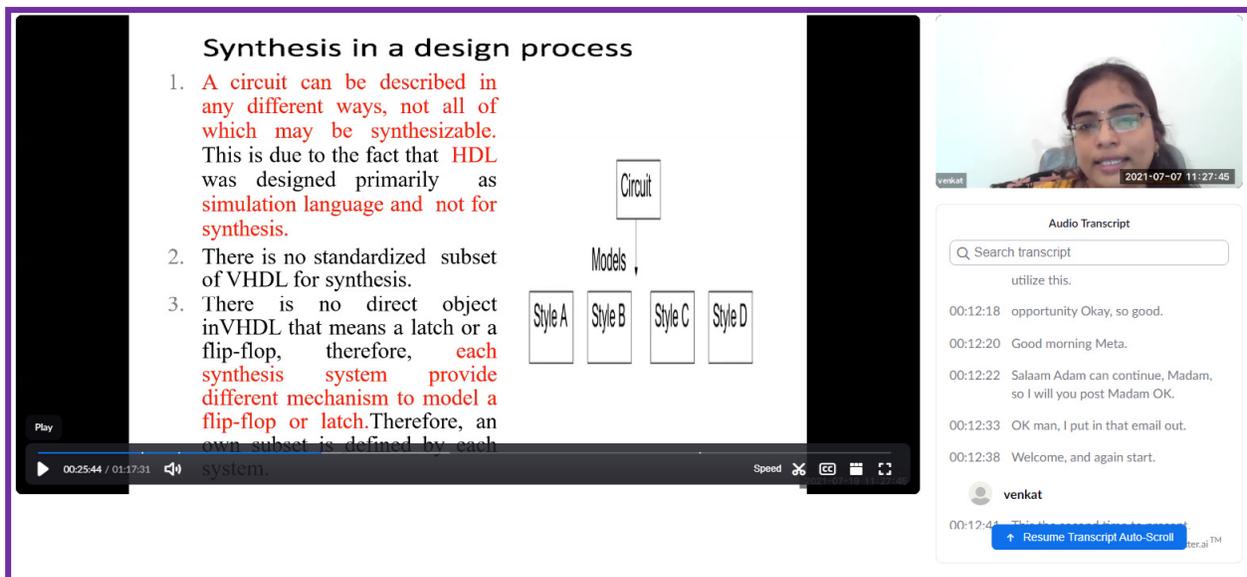
The III B.Tech students from the ECE department had attended this Lecture. Total of **123** students attended to this session.

In this session resource person covered the syllabus which was related to their curriculum. On the first day she started the session by introducing herself and importance of VLSI in present Scenario.



Resource person talking on importance of VLSI

Later she discussed about circuit design flow and synthesis and simulation.

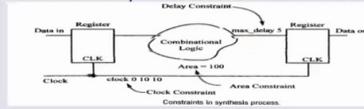


Explaining about synthesis in design process

In the next session she covered subsystem design, counters and high density elements, FPGA and CPLDs.

There are different types of constraints as explained below:

1. Timing constraints:



- These are used to specify maximum delays for particular paths in a design.
- For instance, a typical timing constraint is the required time for an output port.
- The timing constraint guides the optimization and mapping to produce a netlist which meets the timing constraint.
- A typical delay constraint in Leonardo synthesis format is shown below `Set_attribute_port data_out_name required_time_value 25`.
- This constraint specified maximum delay for signal data-out should be less than or equal to 25 library units.

03:26:14 / 03:42:11 Speed [icon] [icon] [icon]

Sarala Gumma

2021-07-12 12:20:28

Audio Transcript

Q Search transcript

- 03:25:53 yeah so I see.
- 03:25:54 associated with MC.
- 03:25:56 MC routing will be very high compared to enter so tool will find out what is the maximum maximum time it has to reach this point and then route it in such a way that this delay is okay that's being done at Daytona beach okay.

Resume Transcript Auto-Scroll

Explaining about Timing Constraints

Students of III B.Tech actively involved in the session where they recollected, related the information and effectively shared their knowledge.

HOD - ECE