NARAYANA ENGINEERING COLLEGE::NELLORE

AUTONOMOUS

Permanently affiliated to JNTUA Ananthapuramu, Approved by AICTE,
Accorded 'A' grade by Govt. of AP, Recognized by UGC 2(f) & 12(B),
ISO 9001:2015 certified Institution, Approved with 'A+' Grade by NAAC

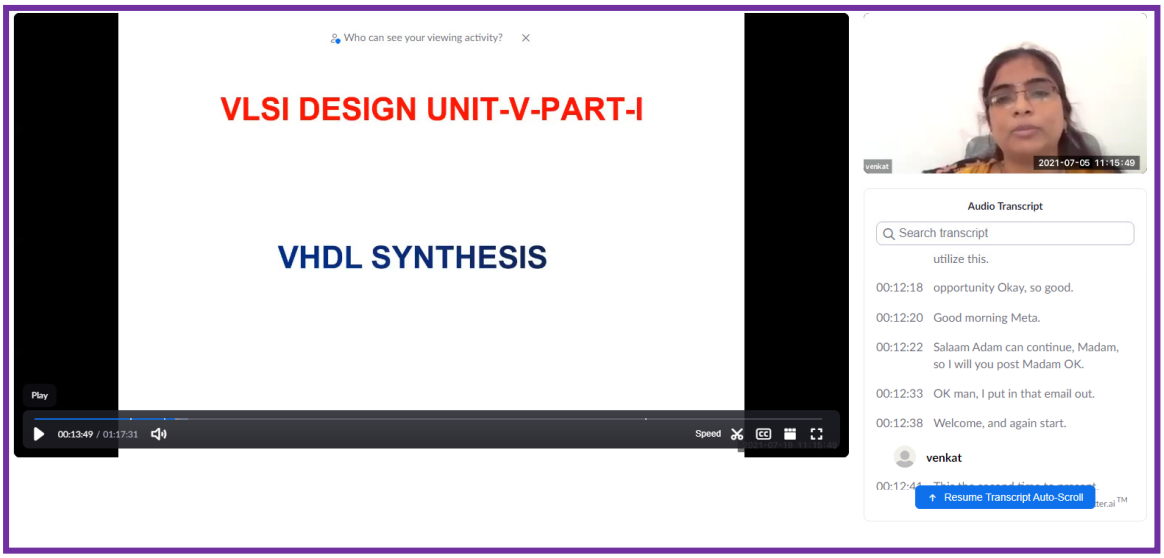
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

1	Name of the Activity/Event	Guest Lecture on " **VLSI Design** "		
2	Date of Activity/Event	**05/07/2021 to 14/07/2021**		
3	Organized by	**Department of Electronics And Communication Engineering**		
4	Place of Activity/event	Online		
5	Resource persons / guest / organization	G. Sarala, Intel corporation, Project lead, Bangalore		
6	Type of activity/Event	Guest Lecture		
7	Activity/Event objectives	• This course aims at providing an opportunity for students to enrich their knowledge and skill in developing various solutions for solving engineering problems in the society. • This program serves as a platform for students to work with the recent trends in Electronic simulation related areas.		
8	Participation	Students	Faculty	Total Participation
		123	-	123
9	General remarks	1. Introduction to VHDL 2. Subsystem design 3. FPGA and CPLDs		
10	Suggested Improvements	Need Hands-on session and more real time examples.		
11	Enclosures	1. Program report with Snapshots 2. Attendance sheet		
12	Signature of Co-ordinator			

The **E**lectronics and **C**ommunication **E**ngineering department has organized a **Guest Lecture** on **"VLSI Design"** from **05/07/2021 to 14/07/2021**, The Resource person is **Mrs. G. Sarala, Intel corporation, Project lead, Bangalore.**

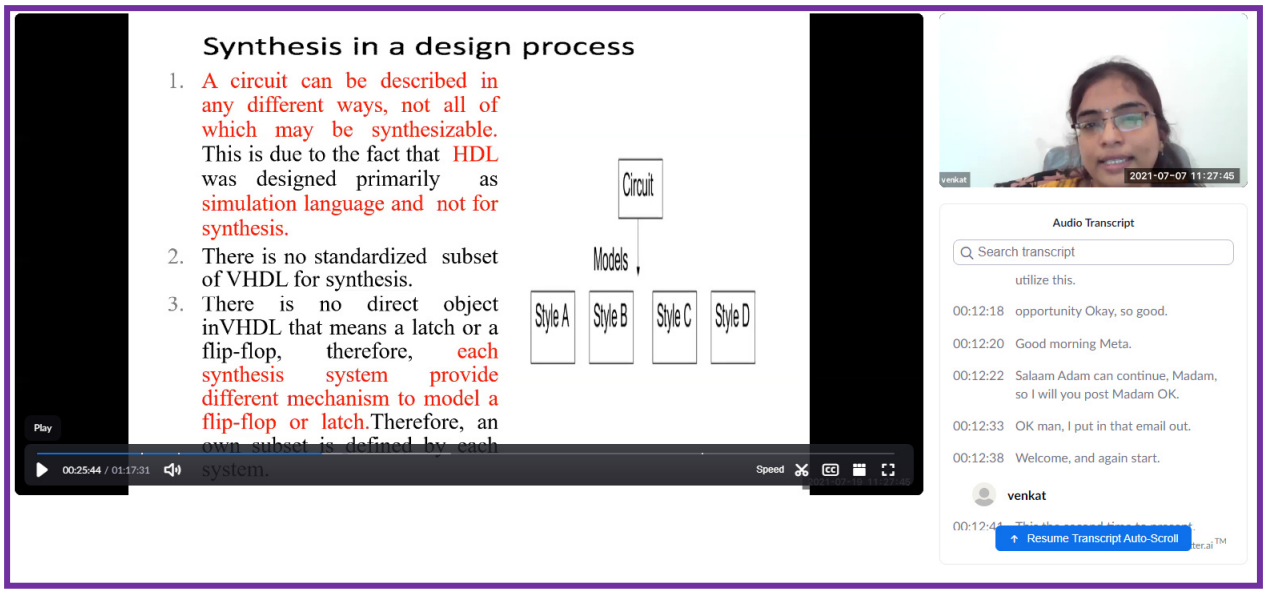
The III B.Tech students from the ECE department had attended this Lecture. Total of **123** students attended to this session.

In this session resource person covered the syllabus which was related to their curriculum. On the first day she started the session by introducing herself and importance of VLSI in present Scenario.



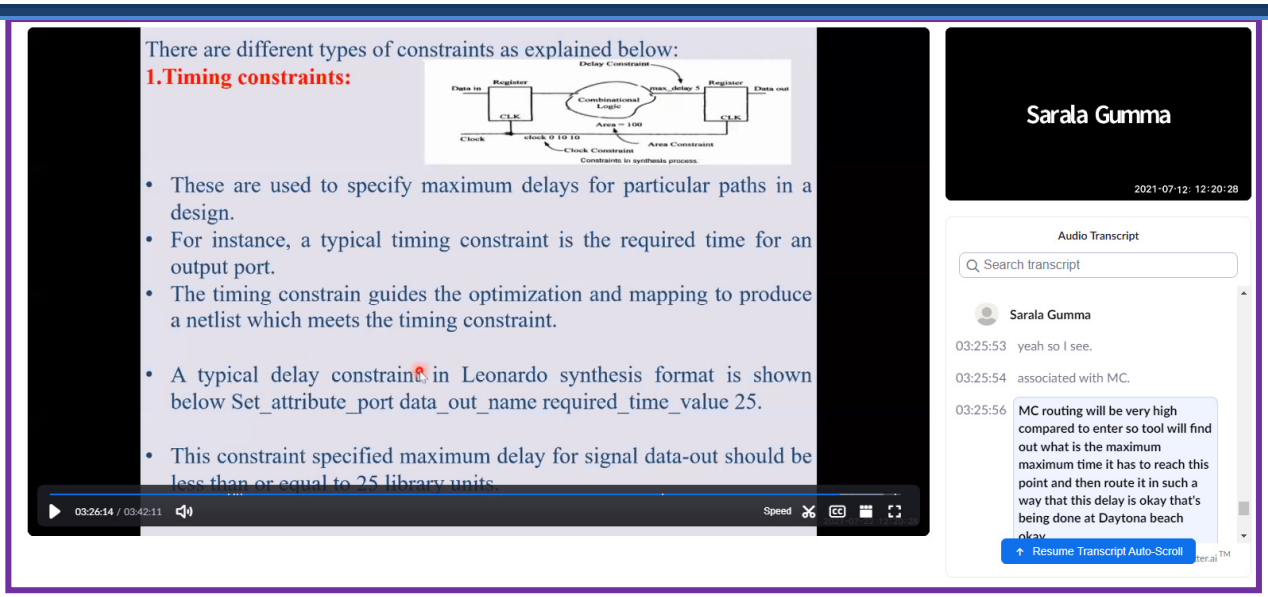
Resource person talking on importance of VLSI

Later she discussed about circuit design flow and synthesis and simulation.



Explaining about synthesis in design process

In the next session she covered subsystem design, counters and high density elements, FPGA and CPLDs.



Explaining about Timing Constraints

Students of III B.Tech actively involved in the session where they recollected, related the information and effectively shared their knowledge.

HOD - ECE